Design of a 3-Stage Decimation Filter for a Sigma-Delta ADC

Otavio Elias V. de Freitas, Edivania F. Silva, Lucas C. Severo, Alessandro G. Girardi,
Crístian Müller and Paulo César C. de Aguirre.
Computer Architecture and Microelectronics Group - GAMA
Federal University of Pampa - UNIPAMPA, Alegrete, Brazil
{otaviofreitas.aluno, cristianmuller, pauloaguirre}@unipampa.edu.br

***Abstract*—This study presents the implementation of a decimation filter for a sigma-delta ADC based on a 3rd-order sigma-delta modulator. The sampling frequency of the sigma-delta modulator is 8 MHz and its bandwidth is 31.25 kHz. The decimation filter consists of three cascade filters: a 4th-order cascaded integrator-comb filter, a compensation finite impulse response (FIR) filter, and a half-band FIR filter. The architecture of the FIR filters seeks optimization of area and power, reducing the use of multipliers. The proposed filter was designed and simulated using the Matlab/Simulink environment considering an ideal bitstream input and ensuring a ripple of only 5 mdB up to 20 kHz.**

***Index Terms*—Sigma-Delta ADC, Cascaded Integrator-Comb, Finite Impulse Response**

I. Introduction

Analog-to-digital converters (ADCs) play an important role on signal processing since they provide an interface between analog and digital worlds [1]. The Sigma-Delta ADC is one of the most used ADC architectures for high-resolution (higher than 14 bits) applications such as industrial instrumentation [2] or audio acquisition [3]. Many consumer electronic devices require audio acquisition systems for communication or voice control. In the last decade, the use of microelectromechanical systems (MEMs) microphones has become a leading solution to the audio module in most portable devices [4]. Sigma-Delta ADCs are adopted in most MEMs microphone systems and the current state-of-the-art MEMS microphones show an SNR ranging from 67 to 69 dB according to [5].

Sigma-Delta ADCs are composed of a sigma-delta modulator (SDM) and a digital decimation filter [6]. The SDM sets the ADC main specifications as the signal-to-noise distortion ratio (SNDR) and the achievable effective number of bits (ENOB). The sigma-delta modulation is based on oversampling and noise-shaping. The noise-shaping effect is responsible for increasing the noise power at high-frequencies, outside the signal bandwidth while removing it from the signal band. To remove this noise, a decimation filter must be employed. This filter is usually composed of a cascaded integrator-comb (CIC) filter followed by one or more finite impulse response (FIR) filters [7]. The purpose of the FIR filters are to compensate for the CIC filter attenuation near the cutoff frequency and to increase the off-band noise removal, providing no signal distortion. Finally, The goal of using more than one FIR filter is to improve the efficiency of the design in terms of area and power consumption when dealing with a hardware implementation.

The main tasks performed by the digital decimation filter are removing quantization noise, decimation, and anti-aliasing [8]. This article presents the design of a 3-stage decimation filter composed of a 4th-order CIC filter, previously designed in [9] and [10], a compensation FIR filter employed to correct the pass-band attenuation due to the CIC filter [11], and a half-band FIR filter to reduce the transition band response, both detailed in this article.

The objective of this article is to show and detail the process of software implementation and optimization of a digital filter, (in this case the sequence of a previously developed CIC filter), in the Matlab/Simulink environment. To validate this project, stimulus data is generated from the simulation of the modulator in Matlab/Simulink.

This paper is organized as follows: Section II explains the continuous-time sigma-delta modulator used as a study case. The decimation filter is presented in Section III. Finally, some conclusions are drawn in Section IV.

II. Sigma Delta Modulator

This work considers the same study case as the one in the previously published paper [9]: A third-order single-bit continuous-time sigma-delta modulator. The modulator simplified diagram is presented in Figure 1. The complete modulator information is also provided in this paper as follows: the coefficients are [c_1, c_2, c_3, a_1, a_2, a_3, g_1] = [1, 1, 1, 0.67, 0.244, 0.044, 0.000361].

The clock signal of this modulator is 8 MHz and the signal bandwidth is 31.25 kHz, leading to an oversampling ratio of

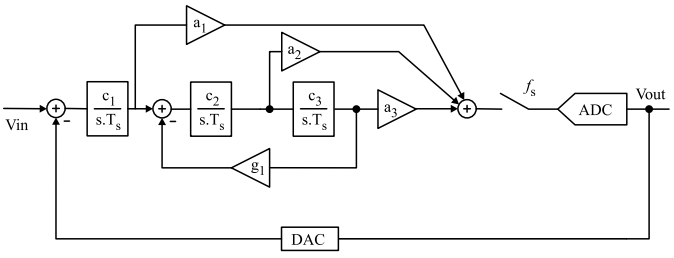

Fig. 1. Third-Order Continuous-Time Sigma-Delta Modulator.

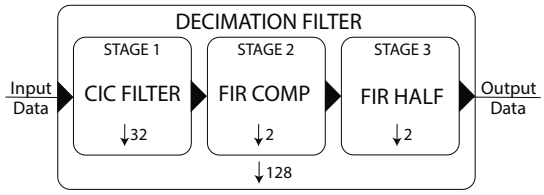

Fig. 2. Decimation Filter Stages.

128. The modulator was simulated with a 1.4038-kHz input signal with an amplitude of -6.02 dBFS. Its output power spectrum density is shown in Figure 5. For the -6.02-dBFS input signal the SNDR is 109 dB and the ENOB is 17.81 bits. The sigma-delta modulator defines the sigma-delta ADC ENOB, and the decimation filter should have a number of bits higher than the modulator ENOB.

The bitstream at the output of this modulator is saved in a text file and used as input stimuli in the decimation filter filter testbench in Simulink.

III. Decimation Filter Design

The decimation filter was designed using three cascaded filters as shown in Figure 2 according to the reference [12]. The decimation filter is designed to have a decimation rate of 128. The first stage of the filter is a fourth-order CIC filter previously designed in [9] and [10]. The transfer function is given by

$$H(z) = \left(\frac{1 - z^{-M}}{1 - z^{-1}}\right)^{L} \tag{1}$$

where M is the decimation factor of the CIC filter and L is the filter order. The CIC filter has the main task of reducing the sampling rate by 32 and giving a gain in the digital word, being of straightforward implementation and efficient.

The second section is a compensation FIR filter, which aims to decimate by 2 and compensate for the magnitude drop in the baseband signal generated by the CIC filter, where the stop frequency is at 90 kHz, with and specific attenuation of 70 dB. The gain of the compensation FIR filter to correct the in-band roll-off of the CIC filter can be seen in Figure 3.

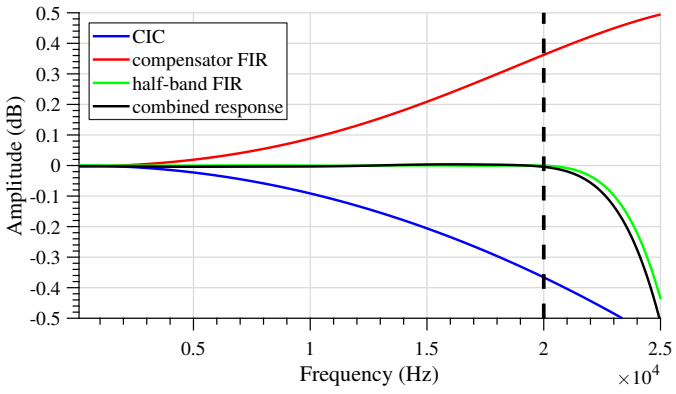

Fig. 3. CIC drop compensation.

The last cascading filter is a half-band FIR filter which aims to provide a sharp transition bandwidth while being cost-effective. This is based on the fact that almost half of the coefficients are zero. This FIR filter also has a decimation rate of 2 and is composed of symmetric coefficients, which ensures a linear phase response. Its stop frequency is at 42.5kHz with an 80 dB attenuation to respect its half-band definition.

TABLE I
FIR FILTER ARCHITECTURE DETAILS

Filter Stage	CIC	Comp	Half-Band	Output
Decimation	32	2	2	128
Samples (kSPS)	250	125	62.5	62.5
Order	4	12	26	-
Group delay (s)	0.48/ODR	1.5/ODR	6.5/ODR	8.48/ODR
Pass-Band (kHz)	-	20	20	20
Stop-Band (kHz)	-	90	42.5	42.5

A. Design of FIR Filters

The designed FIR filter has high-frequency attenuation (low-pass) characteristics. It is represented in the time domain by the convolution between the coefficients and the input data. The coefficients were designed using Matlab, and the input data is the CIC filter output. The equation of the convolution is represented by

$$y(n) = \sum_{k=0}^{N-1} h(k)\, x(n-k) \tag{2}$$

where $h(k)$ is the coefficients of the filter, $x(n-k)$ in the position of the signal at point n, and N is the size of filter coefficients.

The classic FIR filter is built with many multipliers. However, considering a future hardware implementation this work explores the use of only one multiplier. This will reduce the area (and power) overhead in a future silicon implementation.

The details of the filter implemented are shown in Table I. The delay is measured in terms of the output data rate (ODR), which is 62.5 kSPS for this filter.

B. Optimized methods for FIR filter

The conventional architecture of a FIR filter consists of several multipliers that perform the product between the given input data and its coefficients. The method for using only one multiplier consists in organizing all multiplications needed to be performed sequentially over the 128 clock cycles that occurs between each output data. Due to the fact that FIR filters with linear phase response has a symmetrical impulse response, we can reduce by almost half the number of multiplications needed. The described process is represented as follows

$$\sum_{n=1}^{\frac{N}{2}} \beta_n \left(\alpha_n + \alpha_{N-n}\right) \tag{3}$$

where n is an index that sweeps the input data vector of the filter, N is the number of coefficients with non-null values, α

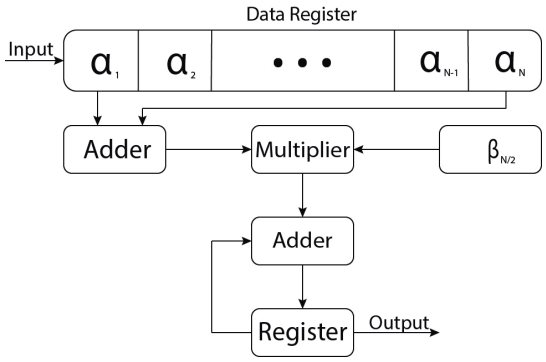

Fig. 4. Optimized FIR Filter

TABLE II
DECIMATION STAGES OF THE DECIMATOR FILTER

Clock Cycles	32	64	96	128
CIC Filter	↓	↓	↓	↓
FIR Comp Filter		↓		↓
FIR Half Filter				↓

is the input data, and β is the coefficients of the FIR filter, respectively.

The described process is represented in Figure 4, where α_N are the filter delays. This strategy will be adopted in future works regarding the filter implementation with hardware description language (HDL). In each clock cycle its values are transmitted to the next register, and the first register receives a new value. The coefficients follow the same logic, but only half of the registers are used due to their symmetrical characteristic.

Table II shows the decimation of the filter throughout its stages, where each arrow means the output of the respective stage. Based on this table it can be seen that for each output data of the entire filter, two outputs are computed for the compensation FIR and one for the half-band FIR. Considering the number of coefficients (order plus 1) in each filter shown in Table I, the total number of sequential multiplications needed is 22. Then, it is possible to use only one multiplier for all multiplications performed by both FIR filters.

For a FIR filter, if the number of coefficients is an even value, only half of the coefficients are used for the multiplications. However, if the number of coefficients are odd, one coefficient lies in the middle of the impulse response and is not duplicated. In the Table I it can be seen that both filters has odd coefficient. While the 13 coefficients of the compensation FIR results in 7 multiplications, the 27 of the half-band FIR results in only 8 multiplications. This low number of filter multiplications is due to the fact that almost half of them are zero.

C. Simulation Results and Filter Response

This subsection presents the digital filter response using a Matlab implementation. Figure 5 depicts the modulator output PSD and the complete decimation filter response. A flat response is verified in-band and the filter roll-of starts around 31.25 kHz. A zoom at in-band frequencies is given in

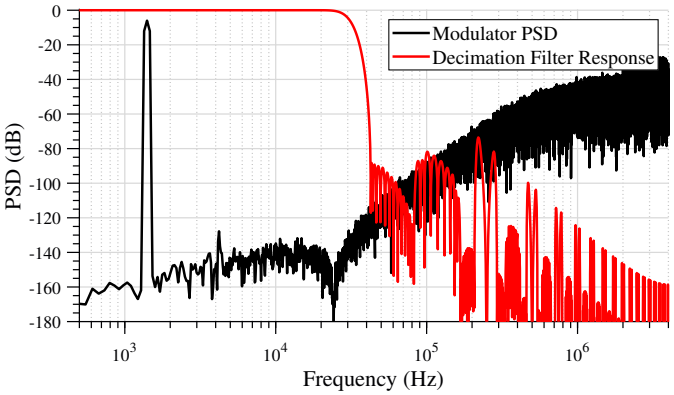

Fig. 5. PSD Bitstream vs Filter Response.

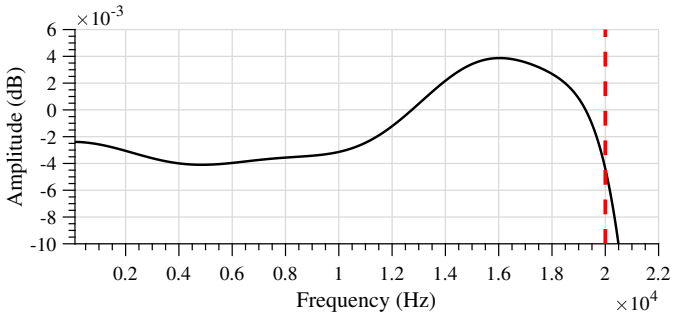

Fig. 6. In-band Ripple.

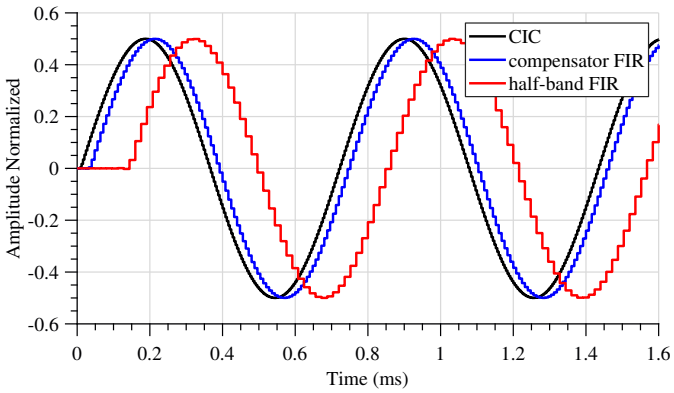

Fig. 7. Digital filter output time-domain response.

Figure 6 to show the filter ripple. A ripple lower than 5 mdB is achieved up to 20 kHz.

For the sake of illustration, the time-domain response of each stage of the decimation filter is depicted in Figure 7. This data is considered a sinusoidal signal with -6.02 dbFS at the ADC input. Finally, Figure 7 shows how significant the half-band stage's group delay is compared to the others, as detailed in Table I.

IV. CONCLUSIONS

This short paper presents the high-level design of digital decimation filter for a sigma-delta ADC with a signal bandwidth of 20 kHz. The designed filter has three stages and can

be implemented with only one multiplier, providing a ripple of 5 mdB within the signal bandwidth. The filter provides a decimation ratio of 128 and its operation was verified by time-domain simulations. In future works, the authors will explore multiplier-less implementations focusing on area and power consumption reduction. Also, the logic and physical synthesis will be performed for future silicon implementation.

V. Acknowledgments

The authors would like to thank FAPERGS process number 22/2551-0000768-6 and Chipus Microelectronics (UNIPAMPA P&D number 31/2022) for supporting this work.

References

[1] F. Maloberti, *Data Converters*. Springer, 2011.

[2] R. Lv, W. Chen, and X. Liu, "A high-dynamic-range switched-capacitor sigma-delta ADC for digital micromechanical vibration gyroscopes," *Micromachines*, vol. 9, no. 8, 2018.

[3] A. Sukumaran and S. Pavan, "Low Power Design Techniques for Single-Bit Audio Continuous-Time Delta Sigma ADCs Using FIR Feedback," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 11, pp. 2515–2525, sep 2014.

[4] P. Malcovati and A. Baschirotto, "The evolution of integrated interfaces for MEMS microphones," *Micromachines*, vol. 9, no. 7, pp. 1–20, 2018.

[5] L. Sant, M. Fuldner, E. Bach, F. Conzatti, A. Caspani, R. Gaggl, A. Baschirotto, and A. Wiesbauer, "A 130dB SPL 72dB SNR MEMS microphone using a sealed-dual membrane transducer and a power-scaling read-out ASIC," *IEEE Sensors Journal*, vol. XX, no. XX, pp. 1–1, 2022.

[6] G. C. T. Richard Schreier, Shanthi Pavan, *Understanding Delta-Sigma Data Converters*, 2017.

[7] S. Parameswaran and N. Krishnapura, *A 100 W Decimator for a 16 bit 24 kHz bandwidth Audio DS Modulator*.

[8] Z. Yigiangl, X. Dongyangl, and Z. Hongliang2, "Optimized design of digital filter in sigma-delta aid converter."

[9] E. Silva, N. Chagas, C. M. Muller, and P. Aguirre, "Design of a Digital CIC Filter for an Audio Sigma-Delta ADC," *Simpósio Sul de Microeletrônica*, 2022.

[10] O. V. E. de Freitas, E. F. Silva, C. Müller, and P. C. C. de Aguirre, "Design of a digital cic filter for an audio sigma-delta adc in the scilab environment."

[11] C. Muller, C. A. Prior, J. B. Martins, P. C. C. de Aguirre, and A. Susin, "A reconfigurable decimation filter design for a cascade 2-2 analog-to-digital converter."

[12] "Analog devices - ad7764 sigma-delta - 24-bit, 312 ksps, 109 db."